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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,998	01/20/2004	Fang-Bin Liu	250210-1040	1645

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
08/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/760,998	LIU, FANG-BIN	
	Examiner	Art Unit	
	Cynthia Britt	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-13 are pending in the present application.

Drawings

The drawings were received on 6/13/07. These drawings are acceptable.

Response to Arguments

Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

Claims 7 8, and 13 are objected to because of the following informalities: the term 'arrays' in these claims should be 'array'. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The following phrase in claim 1 is unclear "wherein the test pattern is processed by the shift register circuit and wherein a particular pattern is produced from the shift

register." The remarks by applicant in the section labeled "b. About the clarity of page 2 in the specification" would indicate that the 'shift register' in question is a linear feedback shift register and not a standard shift register. This is not clear within the claim language.

Claim 8 also recites the following: "wherein a test pattern is input to and processed by the shift register, and then a particular pattern is produced from the shift register". This statement has the same issues as claim 1.

If applicant intends the 'shift register' to be the same as the LFSR recited in the claim, the language of the claim should indicate such. As the claims currently read, there is a LFSR and a separate and distinct shift register. In order to clarify the claim language, applicant is requested to use the same (consistent) terminology for the same items.

The term 'shift register' is typically defined as, a register (made up of sequential latches or flip-flops) in which all bits can be shifted one or more positions to the left or to the right.

The term 'linear feedback shift register' (LFSR) is typicaly defined as a shift register whose input bit is a linear function of its previous state. The only linear functions of single bits are xor and inverse-xor; thus it is a shift register whose input bit is driven by the exclusive-or (xor) of some bits of the overall shift register value. The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the sequence of values produced by the register is completely determined by its current (or previous) state.

Also argued in the above referenced section of the remarks is the fact that these connections are on a circuit board. This is also not clear from the claim language and is not shown in the drawings. If applicant is intending that the LFSR is the interconnect circuit, that also should be in the drawings as these items are unclear to the examiner.

Claims 3, 4, 10, and 11 also seem to have some confusing language in reference to differentiating between 'shift register' and 'LFSR'. The XOR gates could be inherent in LFSR circuitry but may not be in an ordinary shift register.

Claims 2-7 and 9-13 inherit the 35 U.S.C. 112, second paragraph issues of the independent claims by virtue of their dependency. As such, these claims may not be given further consideration with respect to the prior art.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Wells et al. U.S. Patent No. 6,651,238.

As per claims 1 and 8, Wells et al. teach the claimed method and circuitry for testing connections between a first programmable array circuit and a second

programmable array circuit, comprising the steps of: disposing a first connection circuit on the first programmable array circuit according to a preset linear feedback shift register (LFSR) polynomial; disposing a second connection circuit on the second programmable array circuit according to the preset LFSR polynomial, wherein the second connection circuit has a shift register and wherein pins of the second connection circuit are connected to the corresponding pins of the first connection circuit; inputting a test pattern to the shift register, wherein the test pattern is processed by the shift register circuit and wherein a particular pattern is produced from the shift register; and examining the particular pattern to acquire a connection status of the first and the second connection circuits. (Column 6 lines 27-46, column 12 lines 25-57)

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"Testing and Diagnosis of Interconnect Faults in Cluster-Based FPGA Architectures" by Harris et al. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Publication Date: Nov 2002 Volume: 21, Issue: 11 On page(s): 1337- 1343 ISSN: 0278-0070 INSPEC Accession Number: 7462957

This paper teaches that as IC densities are increasing, cluster-based field programmable gate arrays (FPGA) architectures are becoming the architecture of choice for major FPGA manufacturers. A cluster-base architecture is one in which several logic blocks are grouped together into a coarse-grained logic block. While the high-density local interconnect often found within clusters serves to improve FPGA utilization, it also greatly complicates the FPGA interconnect testing problem. To address this issue, we have developed a hierarchical approach to define a set of FPGA configurations which enable interconnect fault detection and diagnosis. This technique enables the detection of bridging faults involving intracluster interconnect and extracluster interconnect. The hierarchical structure of a cluster-based tile is exploited to define intracluster configurations separately from extracluster configurations, thereby improving the efficiency of the configuration definition process. The cornerstone of this work is the concise expression of the detectability conditions of each fault and the distinguishability conditions of each fault pair. By guaranteeing that both intracluster and

extracluster configurations have several test transparency properties, hierarchical fault detectability is ensured.

The examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

The examiner requests applicant to call for an interview before responding to this office action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt
Primary Examiner
Art Unit 2117

Cynthia Britt 8-14-07

CYNTHIA BRITT
PRIMARY EXAMINER

E-BOT OK TO ENTER

In the Drawings

FIGs. 1A and 1B are amended herein by adding the designation of "Prior Art" to the figure labels.

Attachments

Replacement Sheet

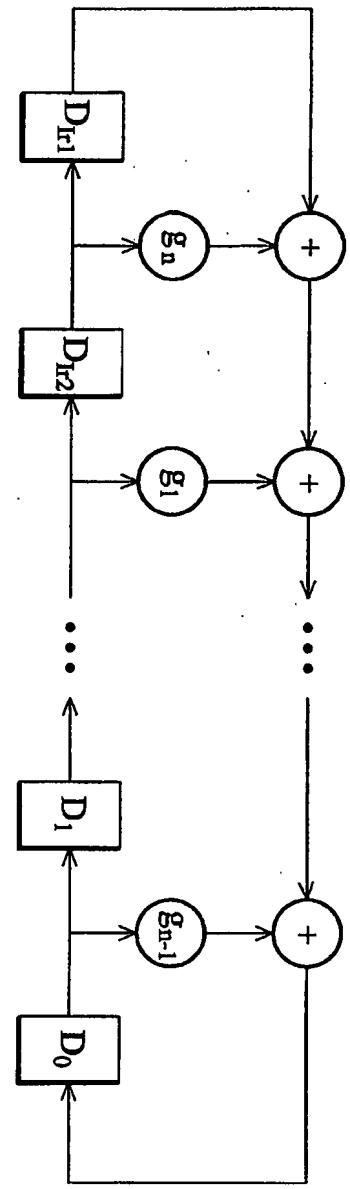

FIG. 1a (PRIOR ART)

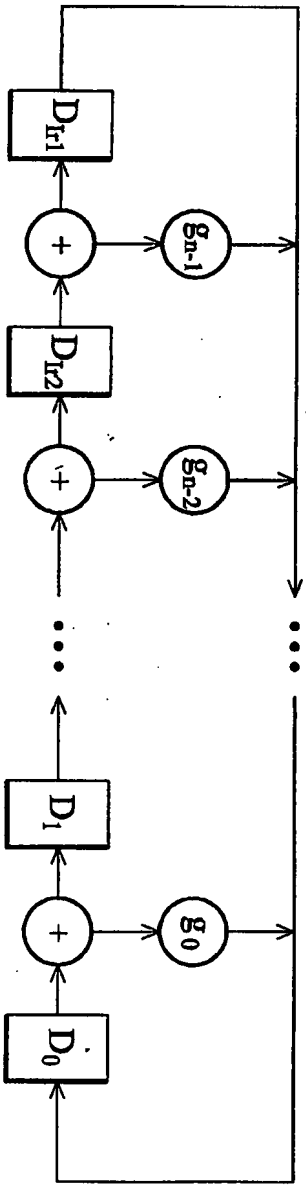

FIG. 1b (PRIOR ART)